What is claimed is:

1. A circuit, comprising:

a receiver for receiving an input train of pulses; and

a delay-locked-loop coupled to an output of the receiver, the delay-locked-loop comprising:

a pulse generator responsive to received input train of pulses produced at the output of the receiver for producing first pulses in response to the leading edges of the received input train of pulses and second pulses in response to the trailing edges of received input train of pulses, the leading edge of the first pulse having the same edge type as the leading edge of the second pulse;

a logic network for combining the first pulses and the second pulses into a composite input signal comprising the first and second pulses with the leading edge of the first pulse maintaining the same edge type;

a variable delay line fed by the composite input signal for producing a composite output train of pulses comprising both the first train of pulses and the second train of pulses after a selected time delay provided by the delay line; and

wherein the delay-locked-loop is responsive to one of the first train of pulses and the second train of pulses in the composite output train of pulses for selecting the time delay of the variable delay line to produce such composite output train of pulses with a predetermined phase relationship with the input train of pulses.

2. The circuit recited in claim 1 wherein the delay-locked-loop includes a phase comparator for producing a control signal for the variable delay line in response to a time difference between pulses in the output train of pulses and pulses in the received train of input pulses.

3. The circuit recited in claim 2 wherein the delay-locked-loop includes a logic network for enabling only one of the first and second pulses to pass from the receiver to the delay line until the phase comparator provides an indication that the output train of pulses have rising edge types timed coincident with both the rising and falling edge types of the input train of pulses.

4. The circuit recited in claim 3 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and

wherein the delay-locked-loop includes:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through such gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

5. The circuit recited in claim 2 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and

wherein the delay-locked-loop includes:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through such gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

6. A circuit, comprising:

a receiver for receiving an input train of pulses;

a pulse generating circuit coupled to an output of the receiver for producing a first pulse in response to a leading edge of each one of the pulses in the input train of pulses and a second pulse in response to the trailing edge of each one of the pulses in the input train of pulses, the leading edges of the first and second pulses having the same edge type;

a variable delay line responsive to the first and second pulses for producing corresponding first and second output pulses, each one of such first and second output pulses being produced in response to the corresponding one of the first and second pulses after a time delay selected in accordance with a control signal fed to the variable delay line;

a phase comparator having a first input fed by one of the first and second pulses and a second input fed by the corresponding one of the first and second output pulses, for producing the control signal, such control signal selecting the time delay for the variable delay line to produce the output pulses with leading edges timed coincident with leading edges of the pulses in the input train of pulses.

7. The circuit recited in claim 6 including:

a logic network for enabling only one of the first and second pulses to pass from the receiver to the delay line until the phase comparator provides an indication that the output train of pulses have leading edges timed coincident with leading edges of the input train of pulses.

8. The circuit recited in claim 7 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through such gate to the phase comparator and to inhibit

feeding the first and second pulses through a delay line to produce the output train of pulses.

13. The method recited in claim 12 wherein the producing step includes producing a control signal for the variable delay line in response to a time difference between pulses in the output train of pulses and pulses in the received train of input pulses.

14. The method recited in claim 13 wherein the producing step comprises enabling only one of the first and second pulses to pass from the receiver to the delay line until an indication is provided that the output train of pulses have leading edges timed coincident with the leading edges of the input train of pulses.

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the output train of pulses from passing through the gate to the phase comparator during the second pulse.

9. The circuit recited in claim 6 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through such gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

10. A circuit, comprising:

a receiver for receiving an input train of pulses such train of pulses having a period, T, such receiver providing a first time delay, Δ_1 to the pulses in the input train of pulses;

a pulse generating circuit coupled to an output of the receiver for producing a first pulse in response to a leading edge of each one of the pulses in the input train of pulses and a second pulse in response to a trailing edge of each one of the pulses in the input train of pulses, the leading edges of the first and second pulses having the same edge type, such pulse generating circuit producing the first pulses and the second pulses with a second time delay Δ_2 after the leading edge of pulses in the input train of pulses;

a logic network for combining the first pulses and the second pulses into a composite input signal comprising the first and second pulses with the leading edge of the first pulse maintaining the same edge type, such logic network providing a third time delay Δ_3 to the first and second pulses;

a variable delay line responsive to the first and second pulses for producing corresponding first and second output pulses, each one of

such first and second output pulses being produced in response to the corresponding one of the first and second pulses after a time delay Δ_L selected in accordance with a control signal fed to the variable delay line;

a delay network fed by the output train of pulses such delay network providing a fourth time delay Δ_4 related to $\Delta_1+\Delta_2$;

a phase comparator having a first input fed by one of the first and second pulses and a second input coupled to an output of the delay network, for producing the control signal, such control signal selecting the time delay Δ_L equal to $nT-(\Delta_1+\Delta_2+\Delta_3)$, where n is an integer to produce the output pulses having leading edges timed coincident with leading edges of the pulses in the input train of pulses.

11. The circuit recited in claim 10 wherein the phase comparator includes a first input fed by pulses in the output train of pulses and a second input fed by pulses in the received train of input pulses and including:

a gate fed by the output train of pulses and a gating signal; and

a gate pulse generator responsive to one of the first and second pulses for producing the gating signal during the first pulse to enable the output train of pulses to pass through such gate to the phase comparator and to inhibit the output train of pulses from passing through the gate to the phase comparator during the second pulse.

12. A method for generating a train of output pulses having a predetermined phase relationship with a train of input pulses, comprising:

passing the input train of pulses through a receiver;

producing a first pulse in response to the leading edge of each the received input train of pulses and a second pulse in response to the trailing edge of each one of the received input train of pulses, each one of the first and second pulses having leading edges with the same edge type;